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Subclass	ISSUE CLASSIFICATION
Class	

PATENT NUMBER

JC1 JC11

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED AA Q.A. ORW	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/551027	D	~~257~~ 438	243	~~2811~~ 2822	

APPLICANTS: Wendell Noble
Leonard Forbes

TITLE: Circuit and method for a folded bit line memory cell with vertical transistor and trench capacitor

PTO-2040 12/99

CPA

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			☐ Continued on Issue Slip Inside File Jacket

☒ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
☒ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. 6,156,604 6,156,607	(Assistant Examiner) (Date)				
	(Primary Examiner) (Date)			ISSUE FEE: Amount Due / Date Paid	
☐ The terminal ____months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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